What Is Claimed Is:

1. A silicon-on-insulator (SOI) semiconductor chip comprising:

a peripheral edge;

a substrate;

an oxide layer on the substrate;

a silicon layer on the oxide layer;

an active area;

an isolation barrier including a groove:

(a) being disposed slightly inward of the peripheral edge of the chip,

(b) extending through the silicon layer and through the oxide layer and partially into the substrate to prohibit impurities in the oxide layer outside the isolation barrier from diffusing into the oxide layer inside the isolation barrier, and

(c) surrounding completely the active area of the chip, and

a passivation layer on the silicon layer and extending to the groove.

2. The SOI chip according to claim 1 wherein the active area of the chip includes a gate located on the silicon layer, a gate metal contact deposited above and forming an electrical contact with the gate, and at least one metal contact deposited above and forming an electrical contact with the silicon layer.

3. The SOI chip according to claim 1 wherein the passivation layer is selected from the group consisting of silicon nitride, polysilicon, oxide, and nitride.

4. The SOI chip according to claim 1 further comprising a barrier material located (i) over the passivation layer on the silicon layer, and (ii) in the groove presenting an additional barrier to impurities in the oxide layer outside the groove from diffusing into the oxide layer inside the groove.

5. The SOI chip according to claim 4 wherein the barrier material is dielectric.

6. The SOI chip according to claim 5 wherein the barrier material is selected from the group consisting of phosphosilicate glass (PSG), BPSG, nitride and oxide.

7. The SOI chip according to claim 1 further comprising the passivation layer on the silicon layer and in the groove.

8. The SOI chip according to claim 7 wherein the passivation layer is selected from the group of silicon nitride, polysilicon, oxide, and nitride.

9. The SOI chip according to claim 7 further comprising an oxide located in the groove and over the passivation layer which is on the silicon layer and in the groove.

10. The SOI chip according to claim 7 further comprising a barrier material located on the passivation layer, over the silicon layer and in the groove, presenting an additional barrier to impurities in the oxide layer outside the groove from diffusing into the oxide layer inside the groove.

11. The SOI chip according to claim 10 wherein the barrier material is dielectric.

12. The SOI chip according to claim 11 wherein the barrier material is selected from the group consisting of phosphosilicate glass (PSG), BPSG, and nitride.

13. The SOI chip according to claim 10 further comprising an oxide located in the groove and over the barrier material and the passivation layer which are in the groove.

14. The SOI chip according to claim 1 wherein the groove is defined by side walls and an open bottom, the SOI chip further comprising the passivation layer on the silicon layer and the side walls of the groove with the bottom of the groove devoid of the passivation layer.

15. The SOI chip according to claim 14 wherein the passivation layer is selected from the group consisting of silicon nitride, polysilicon, oxide, and nitride.

16. The SOI chip according to claim 14 further comprising a fill material deposited in the groove adjacent the passivation layer on the side walls of the groove and contacting the substrate through the open bottom of the groove.

17. The chip according to claim 16 wherein the fill material is polysilicon.

18. The SOI chip according to claim 17 wherein the polysilicon fill material is doped conductive, forming an electrical contact with the substrate.

19. The SOI chip according to claim 18 further comprising a metal contact extending from the doped conductive fill material and forming an electrical contact with substrate.

20. The SOI chip according to claim 1 wherein the groove has a width of about 1-2 microns.

21. A silicon-on-insulator (SOI) semiconductor chip comprising:

a peripheral edge;

a substrate;

an oxide layer on the substrate;

a silicon layer on the oxide layer;

a passivation layer on the silicon layer;

an active area including a gate located above the silicon layer, a gate metal contact located above and forming an electrical contact with the gate, and at least one metal contact located above and forming an electrical contact with the silicon layer;

an isolation barrier, including a groove:

(a) being disposed slightly inward of the peripheral edge of the chip,

(b) extending through the silicon layer and through the oxide layer and partially into the substrate to prohibit impurities in the oxide layer outside the isolation barrier from diffusing into the oxide layer inside the isolation barrier, and

(c) surrounding completely the active area of the chip;

a barrier material located (I) over the passivation layer on the silicon layer, and (ii) in the groove, presenting an additional barrier to impurities in the oxide layer outside the groove from diffusing into the oxide layer inside the groove.

22. A silicon-on-insulator (SOI) semiconductor chip comprising:

a peripheral edge;

a substrate;

an oxide layer on the substrate;

a silicon layer on the oxide layer;

a passivation layer on the silicon layer;

an active area;

an isolation barrier, including a groove:

(a) being disposed slightly inward of the peripheral edge of the chip,

(b) extending through the silicon layer and through the oxide layer and partially into the substrate to prohibit impurities in the oxide layer outside the isolation barrier from diffusing into the oxide layer inside the isolation barrier, and

(c) surrounding completely the active area of the chip;

a barrier material located:

(a) over the passivation layer on the silicon layer, and

(b) in the groove, presenting an additional barrier to impurities in the oxide layer outside the groove from diffusing into the oxide layer inside the groove.

23. The SOI chip according to claim 22 wherein the passivation layer is selected from the group consisting of silicon nitride, polysilicon, oxide, and nitride.

24. The SOI chip according to claim 22 wherein the barrier material is dielectric.

25. The SOI chip according to claim 24 wherein the barrier material is selected from the group consisting of phosphosilicate glass (PSG), BPSG, nitride and oxide that prevents impurities in said oxide layer outside said isolation barrier from diffusing into said oxide layer inside said isolation barrier.

26. The SOI chip according to claim 22 wherein the groove has a width of about 1-2 microns.

27. The SOI chip according to claim 22 wherein the groove in the isolation barrier extends through the passivation layer.

28. A silicon-on-insulator (SOI) semiconductor chip comprising:

a peripheral edge;

a substrate;

an oxide layer on the substrate;

a silicon layer on the oxide layer;

an active area;

an isolation barrier:

(a) including a groove defined by side walls and an open bottom,

(b) being disposed slightly inward of the peripheral edge of the chip,

(c) extending through the silicon layer and through the oxide layer and partially into the substrate to prohibit impurities in the oxide layer outside the isolation barrier from diffusing into the oxide layer inside the isolation barrier, and

(d) surrounding completely the active area of the chip;

a passivation layer on the silicon layer and the side walls of the groove with the bottom of the groove devoid of the passivation layer;

a doped conductive fill material located in the groove adjacent the passivation layer on the sidewalls of the groove forming an electrical contact with the substrate and contacting the substrate through the open bottom of the groove; and

a metal contact extending from the doped conductive fill material and forming an electrical contact with the doped conductive fill material.

29. The SOI chip according to claim 28 wherein the passivation layer is selected from the group consisting of silicon nitride, polysilicon, oxide, and nitride.

30. The SOI chip according to claim 28 wherein the fill material is polysilicon.

31. The SOI chip according to claim 29 wherein the barrier material is polysilicon.

32. The SOI chip according to claim 31 wherein the barrier material is dielectric.

33. The SOI chip according to claim 32 wherein the barrier material is selected from the group consisting of phosphosilicate glass (PSG), BPSG, nitride

and oxide that prevents impurities in said oxide layer outside said isolation barrier from diffusing into said oxide layer inside said isolation barrier.

34. The SOI chip according to claim 31 further comprising an oxide located in the groove and over the barrier material and the passivation layer which are in the groove.

35. The SOI chip according to claim 22 wherein the barrier material is conductive.

36. A silicon-on-insulator (SOI) semiconductor chip comprising:

a peripheral edge;

a substrate;

an oxide layer on the substrate;

a silicon layer on the oxide layer;

an active area;

an isolation barrier, including a groove:

(a) being disposed slightly inward of the peripheral edge of the chip,

(b) extending through the silicon layer and through the oxide layer and partially into the substrate to prohibit impurities in the oxide layer outside the isolation barrier from diffusing into the oxide layer inside the isolation barrier, and

(c) surrounding completely the active area of the chip;

a passivation layer on the silicon layer and in the groove; and

a barrier material located in the passivation layer, over the silicon layer, and in the groove presenting an additional barrier to impurities in the oxide layer outside the groove from diffusing into the oxide layer inside the groove.

37. A silicon-on-insulator (SOI) semiconductor chip comprising:

a peripheral edge;

a substrate;

an oxide layer on the substrate;

a silicon layer on the oxide layer;

an active area;

an isolation barrier, including a groove:

(a) being disposed slightly inward of the pheriphal edge of the chip,

(b) extending through the silicon layer and through the oxide layer and partially into the substrate to prohibit impurities in the oxide layer outside the isolation barrier from diffusing into the oxide layer inside the isolation barrier, and

(c) surrounding completely the active area of the chip.

38. A silicon-on-insulator (SOI) semiconductor chip comprising:

a peripheral edge;

a substrate;

an oxide layer on the substrate;

a silicon layer on the oxide layer;

an active area;

an isolation barrier, including a groove:

(a) being disposed slightly inward of the pheriphal edge of the chip,

(b) extending through the silicon layer and through the oxide layer and partially into the substrate to prohibit impurities in the oxide layer outside the isolation barrier from diffusing into the oxide layer inside the isolation barrier, and

(c) surrounding completely the active area of the chip; and

a passivation layer on the silicon layer and extending to and partially over the groove.